

The diagram illustrates the architecture of the TMS320C49 DSP. It features a central processing core with four 'text ure pipe' blocks. This core is flanked by two 'video' blocks on the left and two 'memory controller' blocks at the bottom. Above the central core, there are two rows of eight 'vp' (video processor) blocks each. The entire system is enclosed within a rectangular frame with a dotted border.

Fig. 1

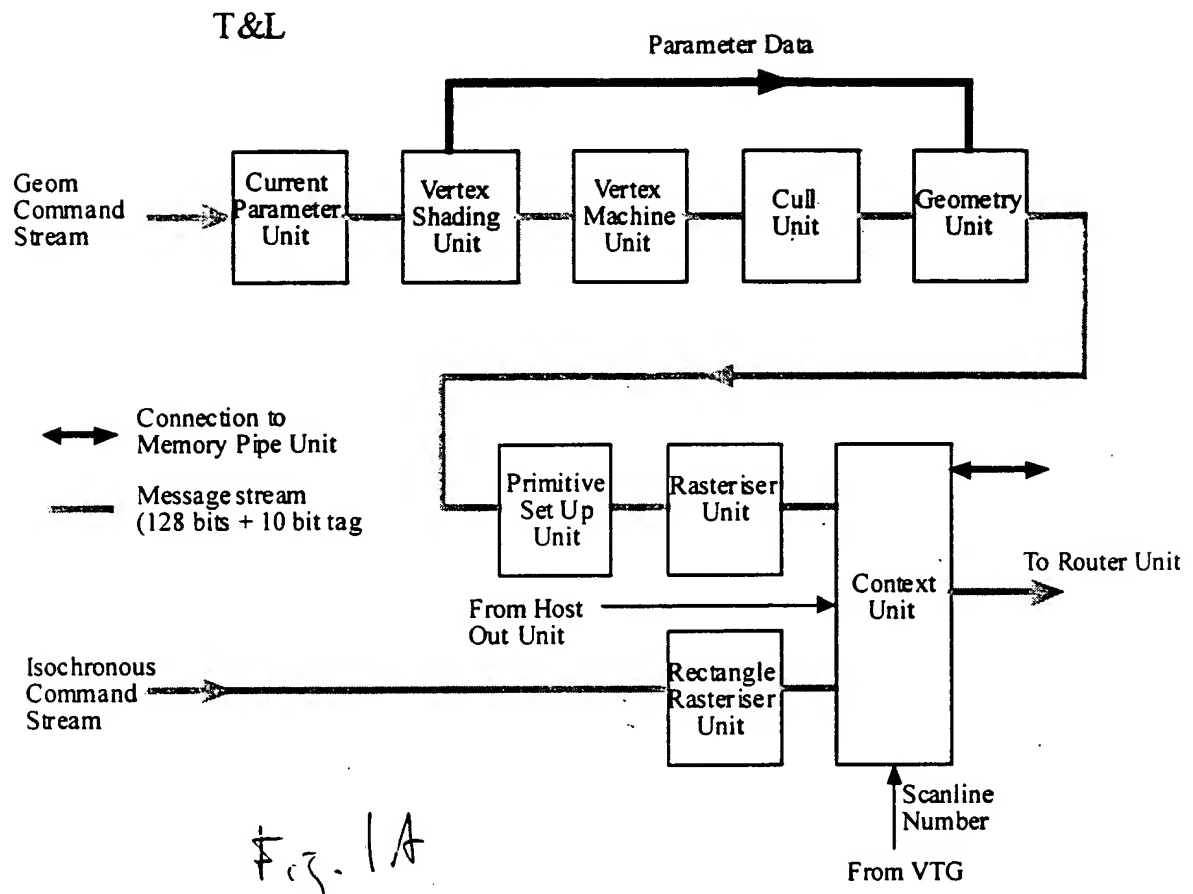
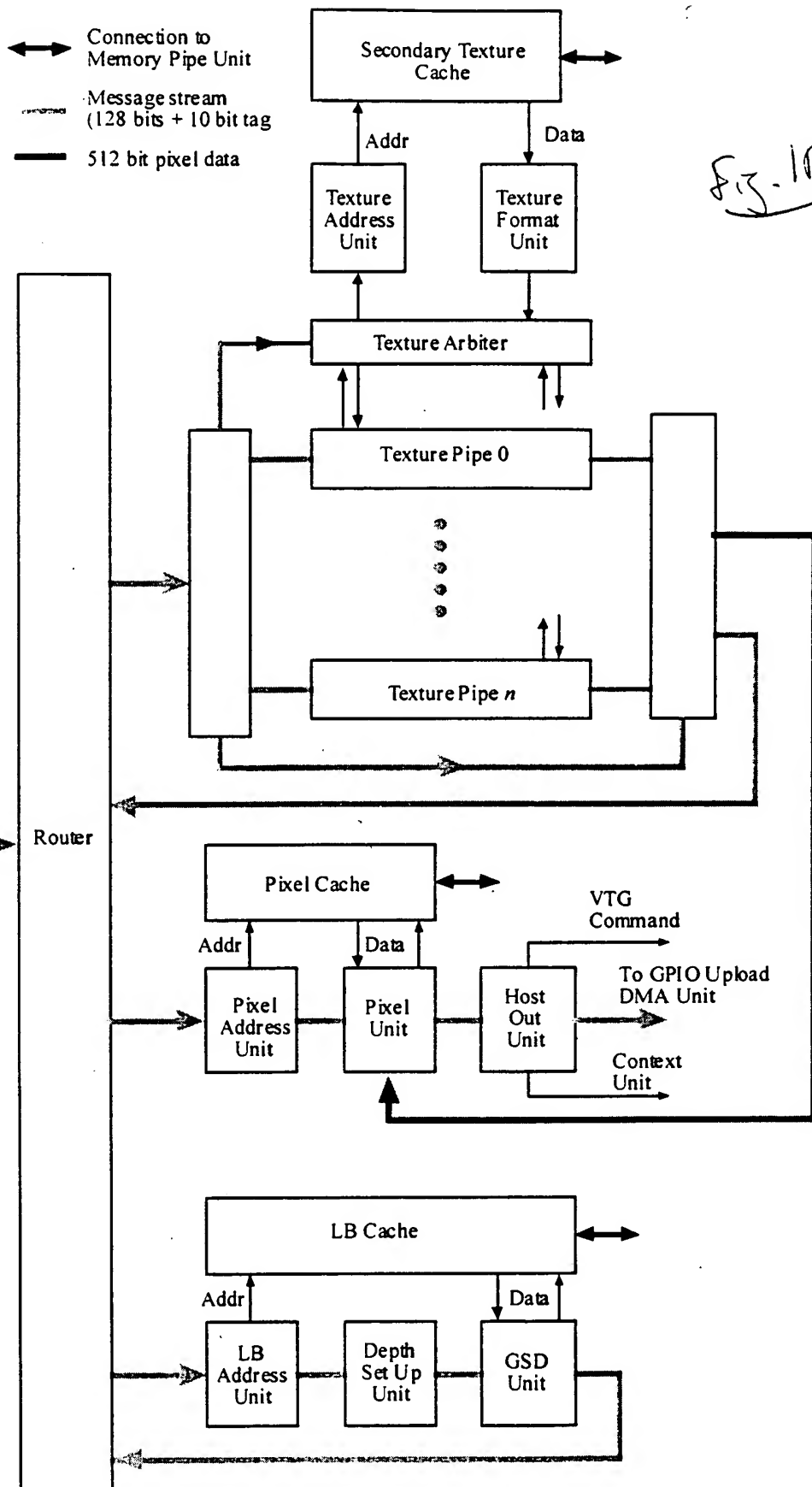


Fig. 1A



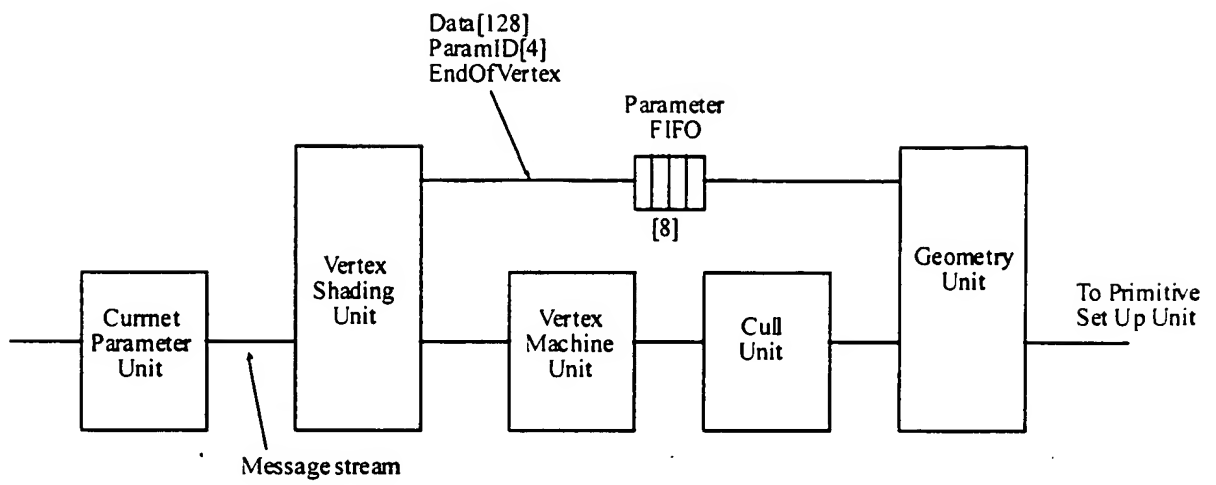
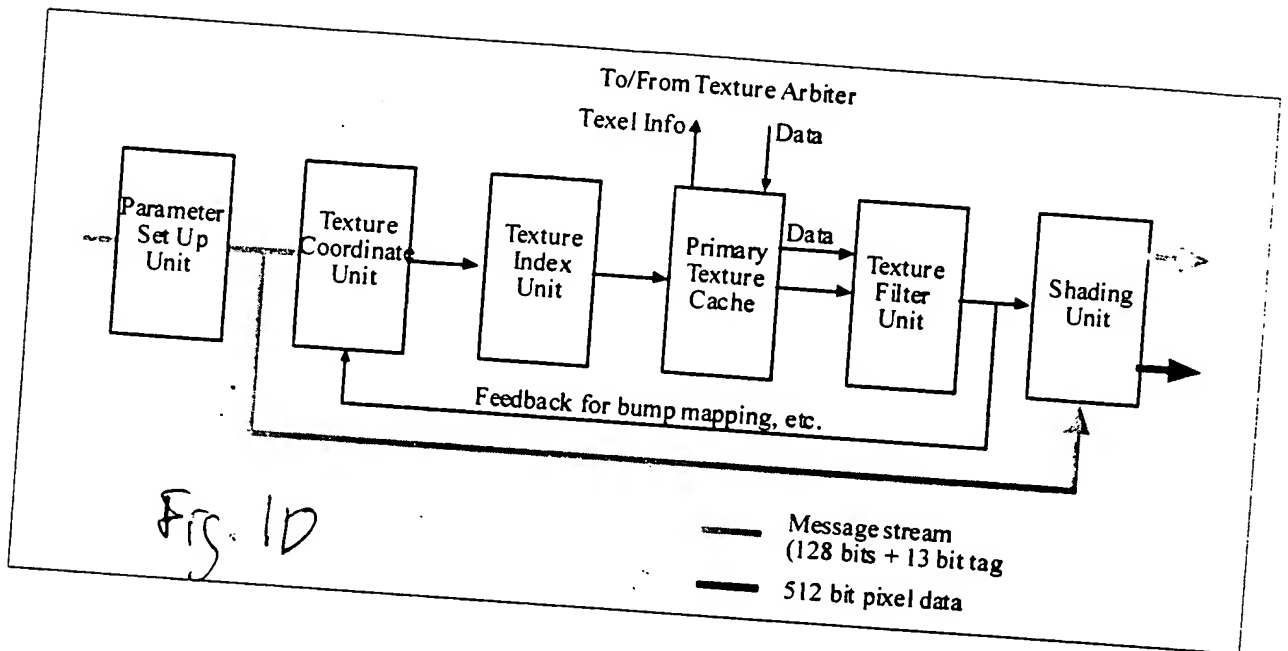
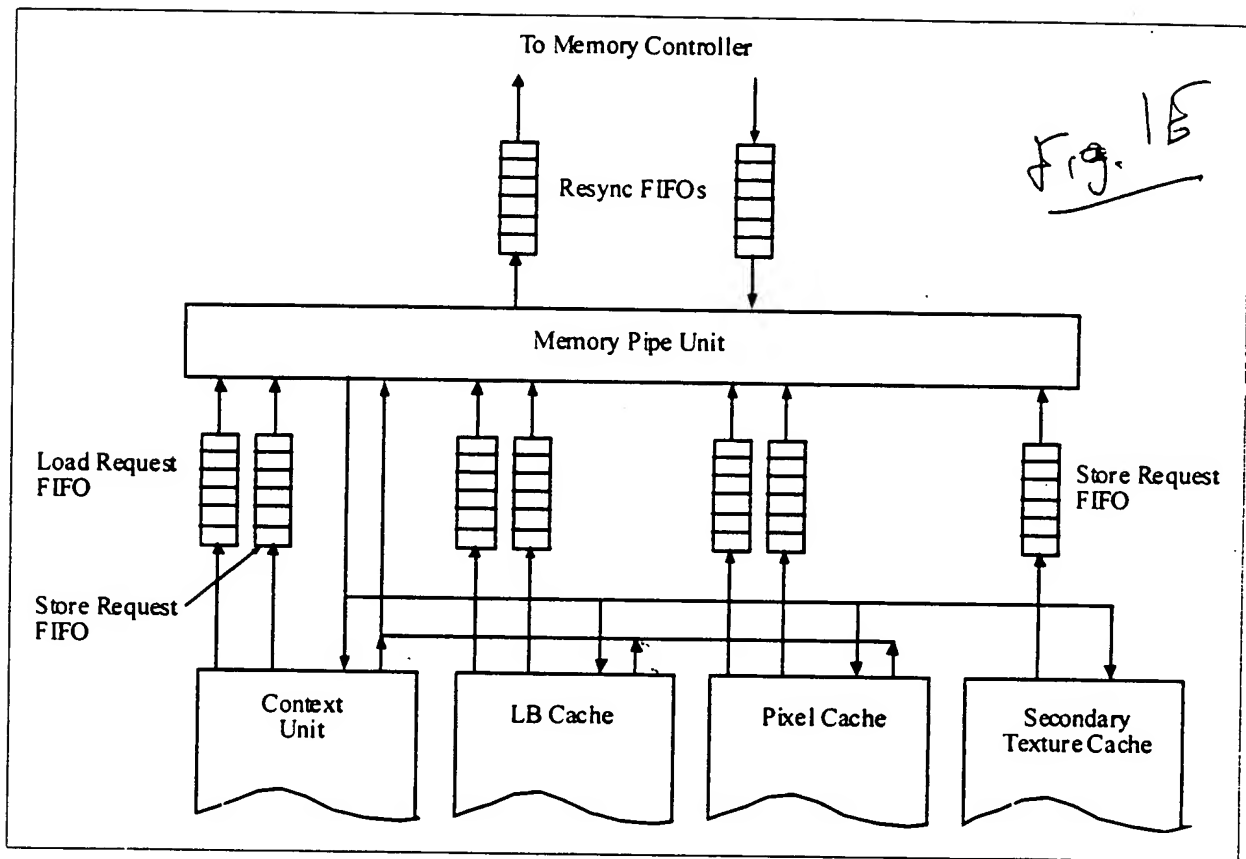


Figure 1c





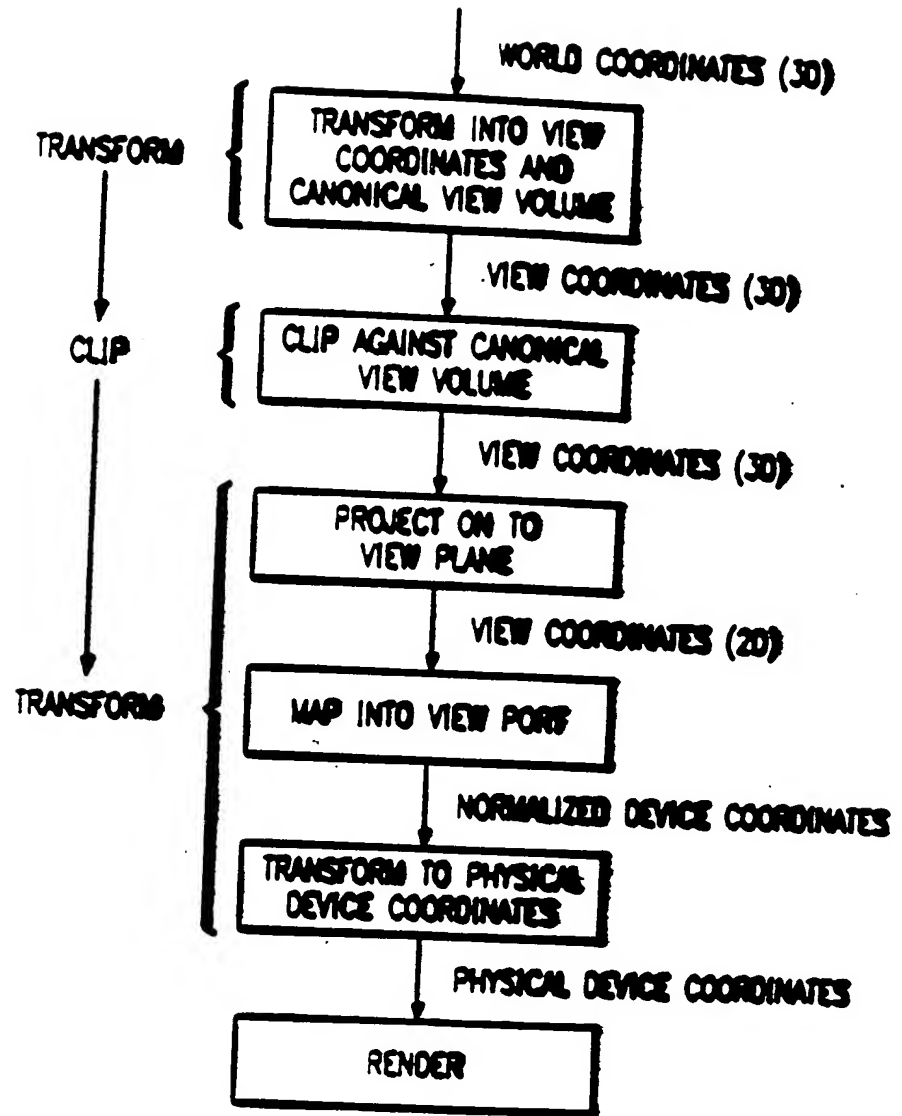


Figure 2